# Architecture and Design of Multiple Valued Digital and Computer Systems

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**Abstract.** Possible architectures and methods for design of multiple valued digital and computer systems are considered in the paper. Different architectures of multiple valued digital and computer systems are proposed and described first. Then algorithm for automated computerized design of such systems is considered and proposed. The algorithm gives possibility for synthesis and optimization of multiple valued digital systems. It is illustrated on example of design of CMOS quaternary multiple valued systems. The method to obtain quaternary CMOS logic circuit is proposed and described. Procedure for optimization of such circuit, according to needed characteristics and concrete operation conditions, is considered and described. The algorithm has been realized on the personal computer and the PSPICE has been used for simulation. Some of computer simulation results confirming described methods and conclusions are given. Example of the algorithm realization is given in the paper.

## 1 Introduction

Digital and computer systems that are practically now used are still mainly binary digital systems. But, some problems that are existing in such systems show possibility and need to use digital and computer systems with the logic basis greater than 2 (so called multiple valued or MV systems and logic) [1-4]. With rapid development of VLSI technologies, the possibilities and reasons for implementation of multiple valued digital and computer systems are becoming real and applicable in parts of a digital system [1-4].

Good characteristics and advantages of multiple valued digital systems and circuits are created great interest for their practical design and implementation [1-4]. There are many advantages of such logic systems and circuits comparing with the binary ones. The main advantages of MV digital and computer systems are: greater speed of arithmetic operations realization, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing [1-4].

From theoretical and practical aspect, the greatest interest exists for and the most investigated, developed and implemented are the ternary (with the logic basis of 3) and quaternary (with the logic basis of 4) MV circuits and systems [1-4]. The first investigated and practically implemented have been ternary MV circuits and systems. Later, the greatest practical interest is for investigation and application of quaternary logic systems and circuits. But, of course, it exists the interest for a general approach for synthesis, design and implementation of multiple valued logic and systems with any logic basis greater than 2. Although in practice still there are not many fully multiple valued digital systems, some parts of a binary digital system are often realized using MV logic [1,2].

The reasons for application and advantages of CMOS technology in binary digital systems and circuits are very well known. All these good characteristics should be also kept in MV logic systems and circuits. There are also some advantages of CMOS technology that are important and characteristic for MV logic. Also, since the first papers about MV logic circuits implementation, the greatest interest exists for implementation in CMOS technology. All these are the reasons that the CMOS technology is the most often used also for design and implementation of multiple-valued circuits and systems.

Possible architectures and methods for design of multiple valued digital and computer systems are considered in the paper. Different architectures of multiple valued digital and computer systems are proposed and described first. Then algorithm for automated computerized design of such systems is considered and proposed. The algorithm gives possibility for synthesis and optimization of multiple valued digital systems. It is illustrated on example of design of CMOS quaternary multiple valued systems. The method to obtain quaternary CMOS logic circuit is proposed and described. Procedure for optimization of such circuit, according to needed characteristics and concrete operation conditions, is considered and described. The algorithm has been realized on the personal computer and the PSPICE has been used for simulation. Some of computer simulation results for one CMOS technology process [5] confirming described methods and conclusions are given. Example of the algorithm realization is given in the paper.

## 2 Architecture of Multiple Valued Digital and Computer Systems

Practically, there are two standard architectures and methods for design of multiple valued digital and computer systems: so called fully MV systems and mixed MV systems [1,2]. Fully multiple valued systems use only MV logic circuits with the same MV logic basis. Mixed MV systems use combination of MV logic circuits and standard binary logic circuits, where a part of the system is realized by using binary logic circuits. Also, very often MV logic is used for realization of some functions inside of binary digital systems [1, 2].

### 2.1 Architecture of Mixed MV Systems

Because of great experience in synthesis, realization and application of binary digital systems, as well because of existing of great number of binary peripheral units, the

binary digital systems will not be easily pushed away from practical use. Especially, very important are high investments in design and production of great number of binary peripheral devices, what is the reason that they will be also further in use. Due to it the mixed multiple valued systems are developed and used. Such systems use two logical bases. Some parts of the system use binary logic circuits with logic basis of 2, and some parts of the system use MV logic circuits with logic basis greater than 2. Binary logic circuits are used mainly for realization of input and output operations, inside of input and output peripheral units and devices. MV logic circuits are used mainly for realization of parts of system for memorizing (operative memory), data processing and data transmission. In such systems it is needed to make conversion of signals from binary system to MV logic system and vice versa, at places where exists connection between of binary system parts and MV system parts.

There are practically two architectures of mixed MV digital computer systems. The two architectures, for MV mixed system with common bus, are shown in Fig.1 and Fig.2.

System in Fig.1 uses binary common bus, binary input and output circuits and units, and one binary part of operative memory. The digital data processing is realized using part of system with greater logic basis R and also part of operative memory is realized using greater basis R. So, in such system, using of greater basis R is limited only on central processing of data and eventually on part of operative memory. Only processing of data is performed with greater logic basis R, and for all other operations the basis 2 is used.

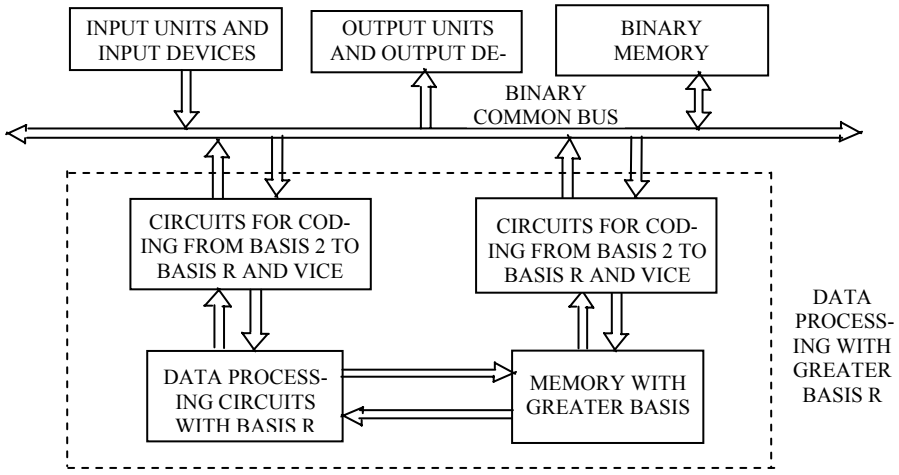


**Fig.1.** Mixed MV digital computer system using binary common bus

Possibility to decrease number of common bus lines, what is great advantage of MV digital systems, creates enormous interest for application of MV common buses. One such mixed MV computer system, using common bus with greater logic basis of R, is shown in Fig.2. In this system greater basis R is used in common bus, in part of data processing logic and in part of operative memory. Input and output units and circuits, part of operative memory and part of data processing logic are binary.

Different variations of this architecture are also possible, first of all depending on what level of data processing is performed using binary and what level using MV logic circuits and devices. One end concerning this architecture will be situation where all logic for central data processing would be binary, and operations with greater basis would be realized only via interconnections between units in the system. In this respect there is certain dilemma among designers reflecting in what extent and for what functions should be introduced operation with greater logic basis and where it should be kept binary circuits and devices.

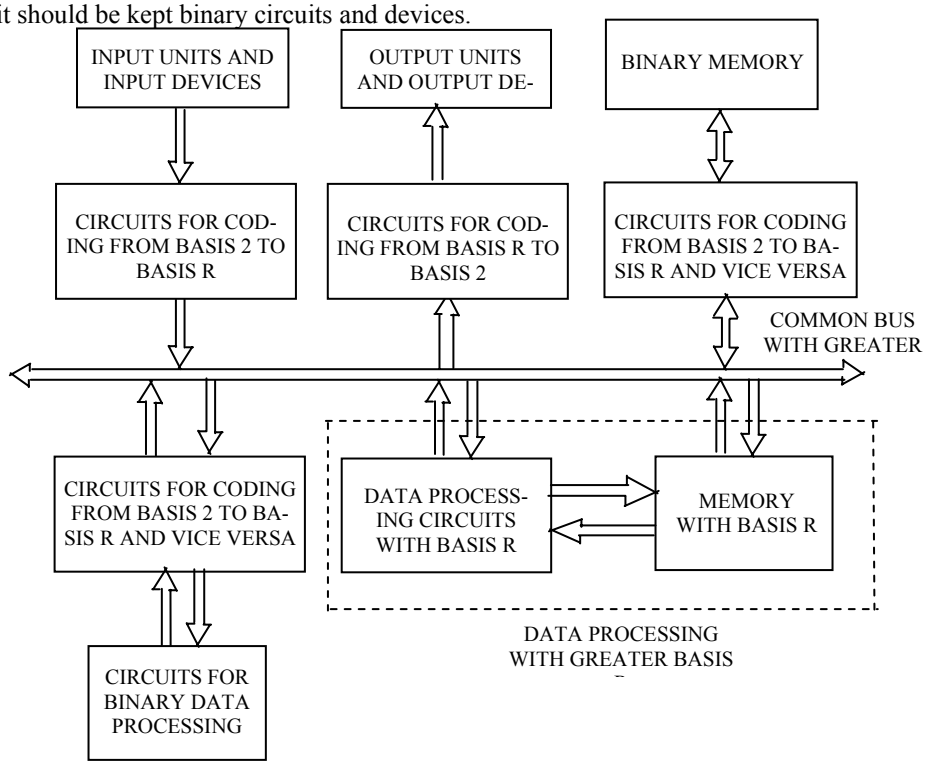


**Fig.2.** Mixed MV digital computer system using common bus with greater logic basis

Circuits in Fig.1. and Fig 2. for coding and decoding from binary system to system with greater logic basis of R, and vice versa, could be considered as well as parts of particular system blocks. These circuits for conversion from basis R to binary basis, and vice versa, are creating great interest of MV digital systems designers. These circuits have been intensively investigated for different logic bases.

## 2.2 Architecture of Fully MV Systems

The fully multiple valued digital systems, as well as binary systems, can be synthesized by more ways and can have different possible architectures, mainly depending on basic logic components used. Such systems can be realized by using max, min and unary operators (circuits), using operators of sum by module and product by module type, using T operators, using multithreshold operators. As an illustration, the princi-

pal realization of MV logic circuit or network with MV max, min and unary operators is shown in Fig.3. This circuit realizes MV logic function of sum of products type. These are architectures of combinational digital systems. There are also other methods of design and architectures of such digital systems, based on using MV spectral techniques, using strongly structured realizations (structures of ROM and PLD type) and using iterative cell matrixes [1,2].

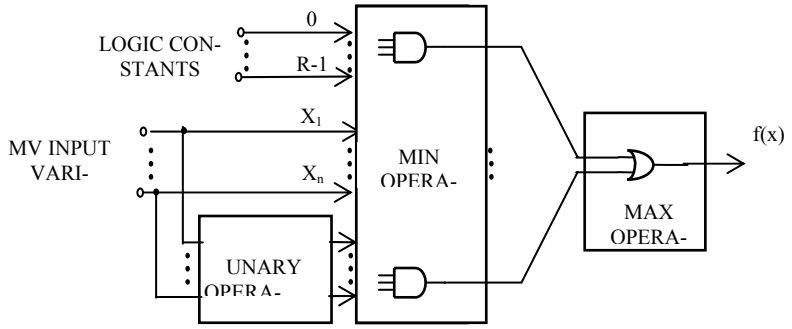


**Fig.3.** Principle of realization of MV combinational logic networks using max, min and unary circuits

Architecture of sequential MV digital systems theoretically can be very similar as architecture of binary sequential systems. General architecture of the binary sequential system can be used for MV sequential systems. Such architecture of MV sequential system with greater logic basis R is shown in Fig.4. The MV sequential system in principle consists of two parts. One part is combinational logic network and the other part is memory elements. The used MV combinational network and MV memory elements are with R logic levels. MV logic signals with R logic states are at the inputs and at the outputs of the system. All the signals inside of the system are also MV logic signals with R logic states. MV logic memory elements with R logic states, so called MV flip-flops, are used as memory elements. Logic states at the outputs of such system depend on logic states at system inputs and logic states at outputs of memory elements. Logic states at output of memory elements are called system state $S_i$. Logic states that are at the inputs of memory elements when the input signals are changing are called next state of system $S_{i,j}$. These states depend on current signals at the system inputs and on previous system state. If the clocked memory elements and the clock signal are used in the system then it is synchronous sequential system. If the clocked memory elements and the clock signal are not used then it is asynchronous sequential system.

## 3 Design of Multiple Valued Digital and Computer Systems

MV logic systems in practice are designed using same methods and procedures as for design of binary systems [1, 2]. The design has a sequence of steps, iterations and interactions. The objective of these activities is, starting from functional requirements of the system, to obtain the system design that can be practically realized as easy as possible. This procedure is realized at more levels of presentation of the system. As

well as in binary system, the solution is represented at tree levels: logic, functional and algorithmic level. Also, at every of solution presentation levels there are tree basic activities: synthesis, optimization and analysis.

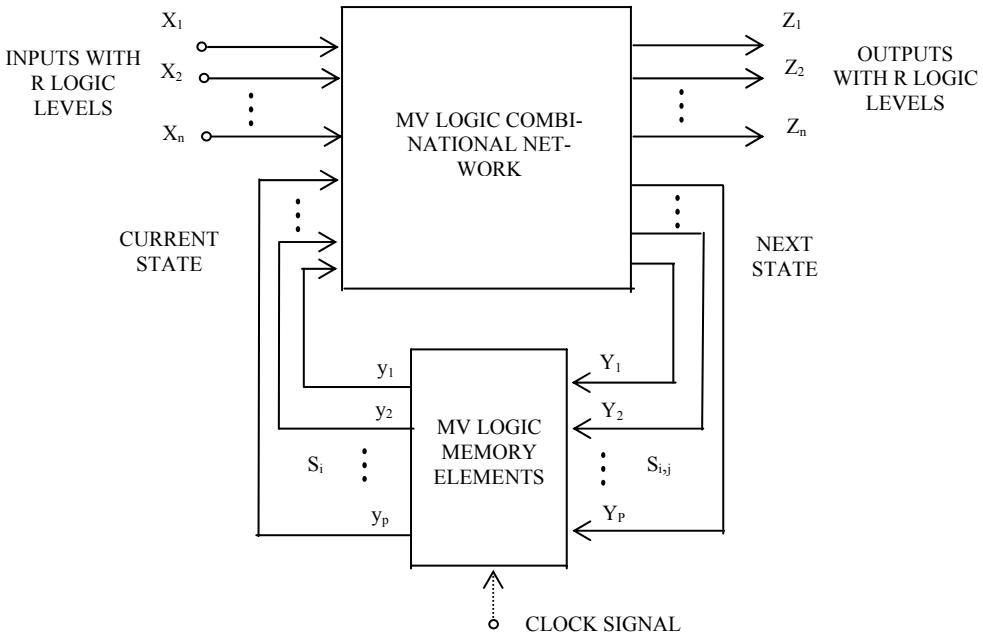


**Fig.4.** General architecture of sequential MV system

Here it will be considered first two activities in design of MV systems: synthesis and optimization. It will be proposed and described method of synthesis and optimization of fully MV system. For analysis it is used PSPICE simulation. The proposed and described procedure of synthesis and optimization has been practically realized for CMOS fully MV quaternary system and will be illustrated on example of such system.

### 3.1 Synthesis of MV Systems

Synthesis of MV digital systems, as well as in binary systems, is realized as a synthesis of logic cells that are used in the system. All the system is decomposed in logic cells and synthesis is performed for each of specific cells. This procedure is still mainly interactive and dependent on experience and skill of designer. In the process first are defined all possible electrical schemes for a certain type of logic cell. This is realized by designer before the design process for all possible logic cells that will be used in the system. Then the selection of electrical scheme for each concrete logic cell is performed. If there are more possible schemes for some type of logic cell then it is performed selection of the scheme that will be optimal at concrete place in the system according to concrete working conditions. That procedure is mainly completely automatised.

Standard procedure for synthesis of MV CMOS digital systems is similar as for binary CMOS systems synthesis. It is synthesis of the logic network using standard CMOS MV logic circuits or cells. The most frequently used standard MV logic circuits for the synthesis are max, min and unary circuits (Fig.3.). The standard CMOS MV logic circuits, i.e. MV CMOS logic cells, should be adequately synthesized and implemented.

One principle for synthesis of CMOS MV digital circuits and systems is proposed here. It enables application of methods used for synthesis of standard binary logic circuits and systems. This principle does not use standard CMOS MV logic circuits. It uses standard CMOS binary logic circuits and appropriate MV CMOS output stage. Such, we obtain more simple procedure for synthesis as well as more simple solutions. The proposed method for the synthesis is shown in Fig. 5.

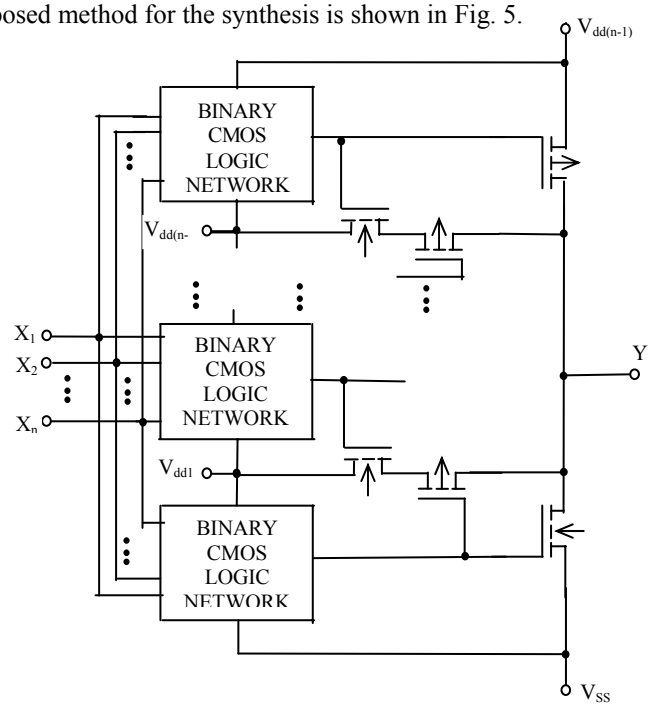


**Fig.5.** Proposed method for synthesis of MV CMOS logic circuits

As it can be seen in Fig.5, the proposed method uses n-1 (where n is equal to logical basis R of used MV system) identical binary CMOS logic networks at the input, conected beetwen diferent supply voltages, and apropriate MV CMOS output stage. The input n-1 binary CMOS networks at the input of circuit define the logic function of whole MV circuit. The CMOS MVoutput stage is controled by n-1 binary CMOS networks and is giving n output states.

The binary CMOS logic networks at the input are realizing the same binary logic function. That binary function is inverse function of the MV output circuit function; i.e. binary function is given by

$$Z = \overline{Y} = \overline{f(X_1, X_2, \ldots, X_n)}, \qquad (1)$$

where Y or f ($X_1$, $X_2$, ... , $X_n$) is the output function that should be realized by the MV circuit.

So, this proposed principle of synthesis of CMOS MV logic circuit or network is based on synthesis of binary CMOS logic networks with binary logic function given by equation (1). Such, we obtain needed MV logic function of realized MV circuit or network. CMOS output stage from Fig. 5 gives n quaternary output levels of whole MV circuit or network with logic basis of n.

Synthesis of input binary logic circuits can be realized in a different ways, first of all depending on used basic binary CMOS circuits. So it can be more different concrete solutions of all MV logic circuit or cell. Next phase in the design is selection of most appropriate solution for concrete working conditions in MV system.

### 3.2 Optimization of MV Systems

Optimization of MV digital systems and circuits, as well as in binary systems, is in essence optimization of MV logic cells or circuits that are previously synthesized and that form MV system. Each logic cell is optimized separately depending of working place and working conditions of the cell in MV system. Working conditions for each logic cell are known: average propagation delay time, fan-out factor, noise immunity, supply voltages. Optimization of logic cell is optimization of cell area with aim to obtain minimal cell area and satisfying working conditions. That optimization procedure depends on used technology process and used MV logic cell. That procedure can be also completely automatized.

The method for optimization of the proposed CMOS MV logic circuits or cells is also proposed and described here. It consists of two procedures: optimization of binary CMOS logic networks at input of MV circuit and optimization of MV CMOS output stage.

The optimization of binary CMOS networks at input of MV circuit can be realized in a similar way as for optimization of CMOS binary circuits since here are used binary CMOS circuits. Here it can be used same principles as for binary CMOS logic circuits. Optimization is performed according to circuit working characteristics and conditions. Here it means that it should determine ratio K of PMOS and NMOS transistor channel width to obtain minimum circuit area and appropriate circuit characteristics. Here proposed criteria is given by

$$F = t_{da} \Delta t_d / NI_R \tag{2}$$

where $t_{da}$ is average propagation delay time, $\Delta t_d$ is absolute difference of edge delays of output signal, $NI_R$ is noise immunity referring to supply voltage. It should minimize value F as a function of ratio K. The ratio K with minimal F is value of K that should be applied in the circuit. Criteria F as a function of ratio K should be obtained by computer simulation.

The task of optimization of CMOS MV circuit output stage is to determine channel widths of output PMOS and NMOS transistors. Optimization is performed according to working conditions of the MV circuit: maximally allowed average propagation delay time, fan-out factor, and supply voltage. The optimization should determine minimal value of ratio $k_o = W_o/W_S$, where $W_o$ is output MOS transistor channel width

and $W_S$ is standard MOS transistor channel width. For real fan-out factor $M_r$ and maximally allowed average propagation delay time $t_{dar}$, approximately can be determined $k_o$ . The procedure of optimization is as follows. First, it should be determined by computer simulation dependence of $t_{da}$ on $k_o$ for known fan-out factor $M_r$ of the MV circuit. Then, it can be determined from the dependence the real ratio $k_o$ what is necessary for the real allowed average propagation delay time $t_{dar}$ of the MV circuit.

# 4 Synthesis and Optimization of CMOS Quaternary Digital Systems and Circuits

Here it will be illustrated the proposed and described procedure for synthesis and optimization of MV digital systems and circuits on example of CMOS quaternary systems and circuits. Some concrete obtained results for some CMOS quaternary logic cells will be shown.

## 4.1 Synthesis of CMOS Quaternary Systems and Circuits

These procedures will be illustrated on the example of synthesis of quaternary CMOS logic cell with a simple quaternary logic function given by

$$Y= f ( X_1, X_2, X_3 ) = X_1 \overline{X}_2 + X_1 \overline{X}_3 . \quad (3)$$

Then it is necessary to realize three identical CMOS binary networks with the same binary function given by

$$Z = \overline{Y} = \overline{X_1 \overline{X}_2 + X_1 \overline{X}_3} . \quad (4)$$

So, this principle is very simple. The three binary CMOS logic networks at the input of quaternary circuit are realized identicaly using standard CMOS binary logic circuits. So, the same methods as for synthesis of binary logic circuits are used here for synthesis of quaternary logic circuits. That is the advantage of this principle of synthesis.

There are possibilities to obtain different binary CMOS logic networks, depending of the basic binary circuits used and methods used for optimization of scheme of binary logic network. In the synthesis it is needed and necessary to use all methods for minimization used in binary digital systems synthesis. In Fig.6 it is given illustration of two possible synthesis of the circuit with logic function given by equation (3). If it is used relation (4) for synthesis then it will be obtained circuit shown in Fig.6a. But, if it is used possibility for transformation and minimization of binary function given by equation (3) then it could be obtained other form of the same function given by

$$Z = \overline{X_1 \ \overline{X_2 \ X_3}} . \quad (5)$$

If this form of the logic function is used for synthesis then it will be obtained solution shown in Fig.6b.

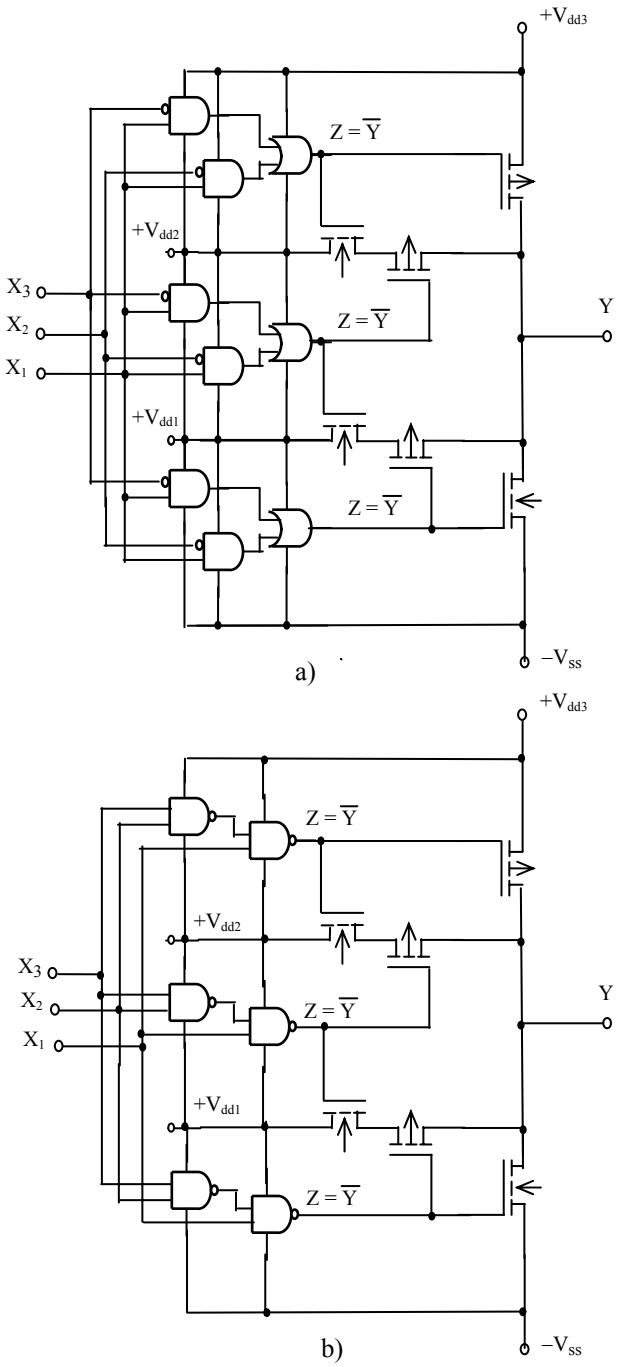


**Fig.6.** Solutions of quaternary CMOS circuit with logic function given by eq. (3)

It can be concluded that the circuit in Fig.6b is simpler. It uses less number of transistors and has less average propagation delay time than the solution in Fig.6a. The conclusion about less average propagation delay time of the circuit in Fig.6b has been verified by PSPICE simulation. So, circuit given in Fig.6b will be selected as the solution for CMOS quaternary logic cell with logic function given by equation (3).

Circuits in Fig.6 have simple logic function and are very simple solutions. But, the some procedure of synthesis and all benefits of this method are applicable also for more complex CMOS quaternary logic functions and logic cells synthesis.

### 4.2 Optimization of CMOS Quaternary Systems and Cells

Here it will be shown some results of optimization of CMOS quaternary logic cell given in Fig.6.b. It will be shown results obtained for optimizations of input CMOS binary networks and for optimization of CMOS quaternary output stage.

Dependence of criteria F on ratio K for quaternary CMOS circuit from Fig. 6b, obtained by PSPICE simulation, is shown in Fig. 7. From the dependence in Fig.7 it should be selected ratio K for what criteria F has minimal value.

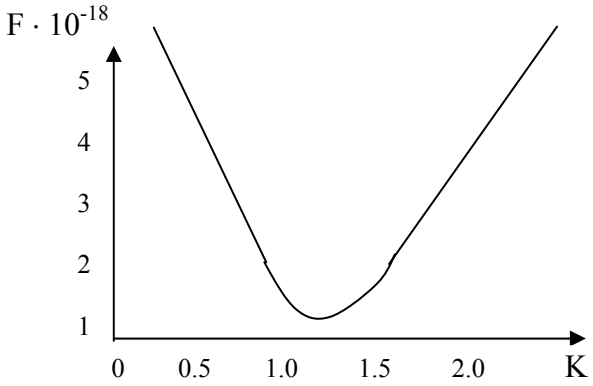


**Fig.7.** Criteria F as a function of ratio K for quaternary CMOS circuit in Fig.6b

The optimization of CMOS quaternary circuit output stage should determine minimal value of ratio $k_o = W_o/W_S$ of output MOS transistor channel width and standard MOS transistor channel width for what the circuit will satisfy its needed characteristics at concrete working conditions. For real fan-out factor $M_r$ and maximally allowed average propagation delay time $t_{dar}$, it can be approximately determined $k_o$. The way of this optimization is principally shown in Fig. 8. The average propagation delay time $t_{da}$ as a function of $k_o$ for fan-out factor $M_r$=5, obtained by PSPICE simulation, is shown in Fig. 8.

The procedure of optimization is as follows. First, it should be determined by computer simulation dependence of $t_{da}$ on $k_o$ for known fan-out factor $M_r$ of the CMOS quaternary circuit. That dependence for circuit in Fig.6b is shown in Fig. 8. Then, it can be determined from the dependence the real ratio $k_o$ what is necessary for the real allowed average propagation delay time $t_{dar}$ of the quaternary circuit. Then it

should be selected the closest greater possible value of ratio $k_o$ as a value of $k_o$ that will be practically used. To make the procedure shorter and quicker it is enough to perform circuit simulation only for real fan-out factor $M_r$ and for different values of ratio $k_o$ until it will be obtained the first possible $k_o$ value for what it will be $t_{da}$ less than $t_{dar}$ . It has been illustrated by dashed line in Fig. 8.

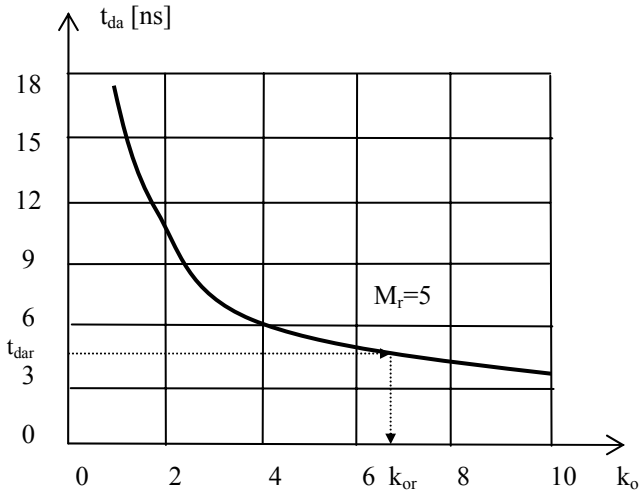


**Fig.8.** Average propagation delay time as a function of $k_o$ for circuit in Fig.6b

All given simulation results have been obtained by PSPICE computer simulation for parameters of one CMOS technology process [5] and supply voltages $V_{SS}$ = 0V, $V_{dd1}$ = 3V, $V_{dd2}$ = 6V, $V_{dd3}$ = 9V

## 5 Conclusions

The proposed and described architectures of MV digital systems and computers give the possibility for design of appropriate MV system depending on the need of user. There are certain possibilities that are applicable and appropriate for different needs and working conditions.

For design and realization of MV logic circuits and systems practically are used similar or the same metodes and procedures which are used also in the binary logic circuits and systems. One of the most important procedures in design of MV logic circuits is synthesis and optimization. Here proposed and described algorithm of synthesis and optimization enables automatization of design and obtaining of logic circuits with minimal circuit area with fullfiling needed characteristics. It is iterative and interactive process which is realized by personal computer. In principle, it can be used for all types of logic circuits and for all technologies of circuit manufacturing. It has been practicaly realized and intended for synthesis and optimization of CMOS MV quaternary logic circuits and systems.

The proposed methods and procedures for synthesis and optimization of quaternary electronic digital circuits and systems are very simple.

The synthesis is based on synthesis of binary logic networks since it is necessary to synthesize CMOS binary logic networks at the input of quaternary circuit. So, same methods as for binary CMOS logic circuits synthesis are also used here. So, it can be easily realized CMOS quaternary circuit with any output function.

Optimization is based on optimization of input CMOS binary circuits and optimization of quaternary CMOS output stage. The procedures are very similar as in binary CMOS circuits optimization and design.

The proposed procedures are very suitable for realization using computer, as iterative and interactive procedures. Practically the procedures have been realized by personal computer. PSPICE has been used for simulation of circuits.

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